BOXER-6642-CML

Fanless Embedded Box PC

User's Manual 1st Ed

Last Updated: April 7, 2021

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● BOXER-6642-CML	1
● Wallmount bracket	2
● Screw Package	1
● 3 Pin DC-In Power Connector	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any power supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls.
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. Do not leave this device in an uncontrolled environment with temperatures beyond the device's permitted storage temperatures (see chapter 1) to prevent damage.
19. Do NOT disassemble the motherboard so as not to damage the system or void your warranty.
20. If the thermal pad had been damaged, please contact AAEON's salesperson to purchase a new one. Do NOT use those of other brands.
21. The Hex Cylinder Coppers on the front panel are not removable.
22. Repeatedly assemble and disassemble the system may cause damages to the exterior paint and surface and screw holes.
23. Use the right size screwdriver.
24. Use the screwdriver correctly to remove screws from the system.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚(PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	×	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

备注:

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Hazardous and Toxic Materials List

AAEON System QO4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated biphenyls (PBBs)	Polybrominated diphenyl ethers (PBDEs)
PCB and Components	X	O	O	O	O	O
Wires & Connectors for Ext.Connections	X	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	X	O	O	O	O	O
HDD Drive	X	O	O	O	O	O
LCD Module	X	X	O	O	O	O
Optical Drive	X	O	O	O	O	O
Touch Control Module	X	O	O	O	O	O
PSU	X	O	O	O	O	O
Battery	X	O	O	O	O	O

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
CPU	Intel® Core™ i9-10900TE Intel® Core™ i7-10700TE Intel® Core™ i5-10500TE Intel® Core™ i3-10100TE Intel® Celeron® G5900TE
Chipset	Intel® Q470E
System Memory	DDR4-2666 So-DIMM slot x 2, up to 64GB
Display Interface	HDMI x 1
Storage Device	2.5" SATA HDD/SSD Bay x 1 M.2 2280 for NVMe SSD
Ethernet	Intel® i211 x 1 Intel® i219 x 1
I/O	HDMI x 1 RJ-45 x 2 for GbE LAN (i211 x 1, i219 x 1) USB 3.2 Gen 1 x 4 USB 2.0 x 2 DB-9 x 4 for RS-232/422/485 Line out x 1 3-pin 10~35V Power Input x 1 Power Button x 1
Expansion	M.2 2230 E Key x 1 M.2 2280 M Key x 1 Full-Size Mini Card x1 (mSATA/PCIe switch by BIOS, default PCIe) SIM x 1
Indicator	N/A
OS Support	Windows® 10 IoT Enterprise 64-bit Linux Ubuntu 20.04

Power Supply

Power Requirement	3-pin DC Input 10~35V

Mechanical

Mounting	Wall mount
Dimensions (W x H x D)	11.5" x 2.1" x 6.0" (292.4mm x 53.5mm x 152mm) w/o bracket
Gross Weight	6.2 lbs. (2.8 kg)
Net Weight	8.4 lbs. (3.8 kg)

Environmental

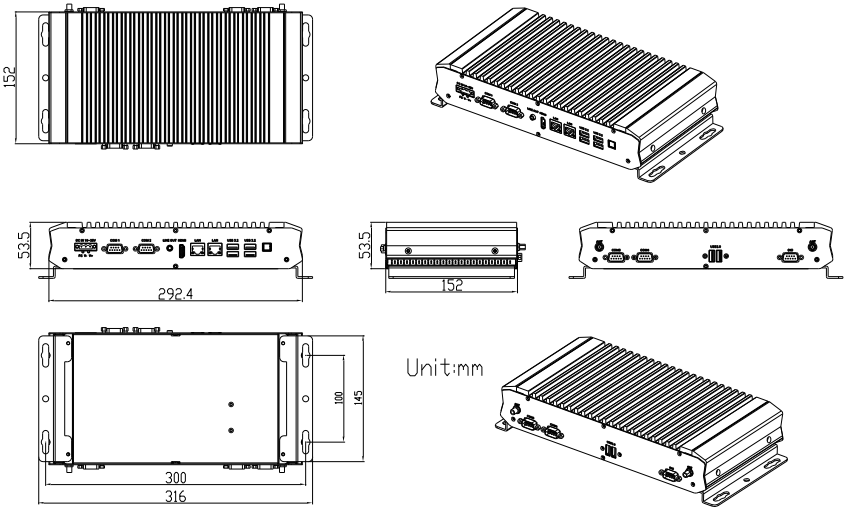
Operating Temperature	32°F ~ 113°F (0°C ~ 45°C) with 0.5 m/s airflow with TDP ≤ 35W CPU
Storage Temperature	-40°F ~ 176°F (-40°C ~ 80°C)
Storage Humidity	5 ~ 95% @ 40°C, non-condensing
Anti-Vibration	2 Grms/ 5 ~ 500Hz/ operation with SSD/mSATA 1 Grms/ 5 ~ 500Hz/ operation with HDD
Certification	CE/FCC Class A

Chapter 2

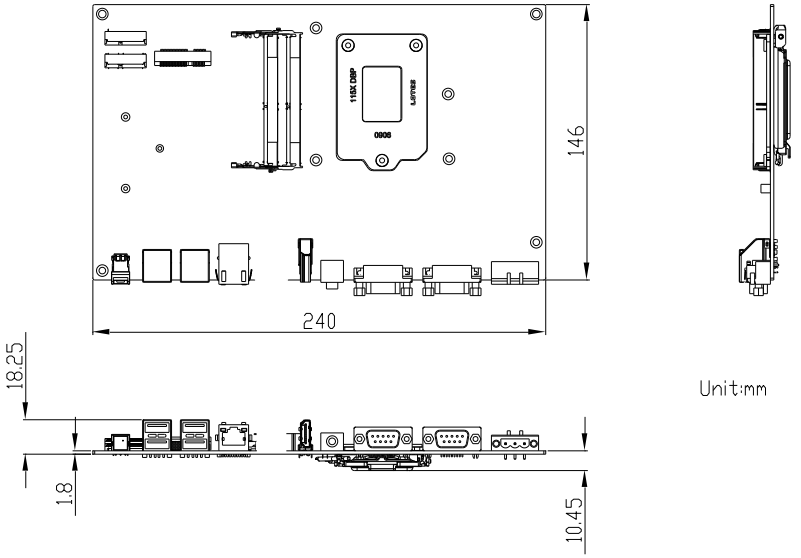
Hardware Information

2.1 Dimensions

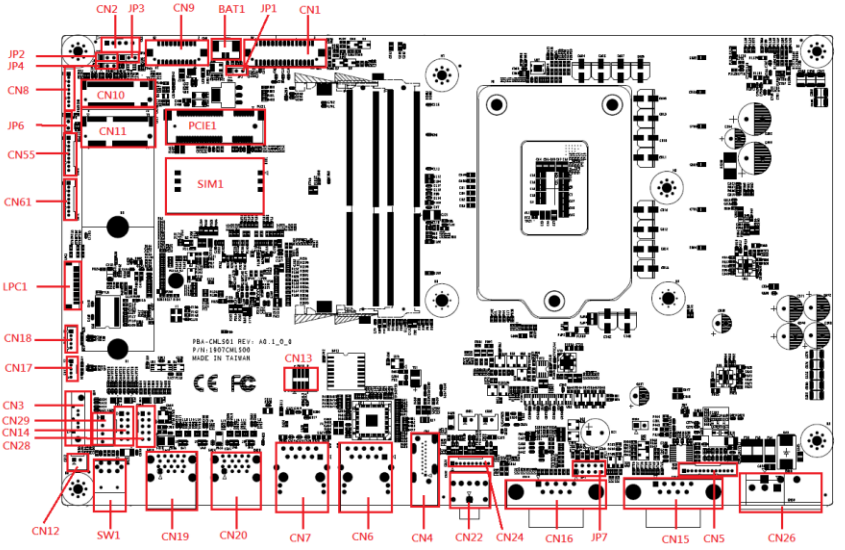
System



Board Dimensions



2.2 Jumpers and Connectors

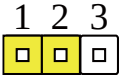


2.3 List of Jumpers

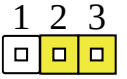
Please refer to the table below for all of the system's jumpers that you can configure for your application

Label	Function
JP1	Clear CMOS
JP2	LVDS BKLT Power
JP3	LVDS BKLT Control Selection
JP4	4,5,8 Wire Selection
JP6	Auto Power Button Selection

2.3.1 Clear CMOS (JP1)

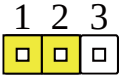


Normal (**Default**)

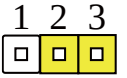


Clear CMOS

2.3.2 LVDS BKLT Power (JP2)

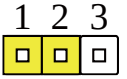


12V

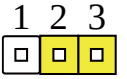


5V (**Default**)

2.3.3 LVDS BKLT Control Selection (JP3)

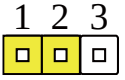


VR Mode

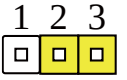


PWM Mode (**Default**)

2.3.4 4,5,8 Wire Selection

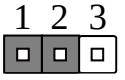


4,8 Wire

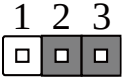


5 Wire (**Default**)

2.3.5 Auto Power Button Selection (JP3)



ATX (**Default**)



AT

2.4 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

Label	Function
CN1	LVDS Port
CN2	LVDS Inverter
CN3	SATA Port
CN4	HDMI Port
CN5	VGA Port (Wafer)
CN6	LAN RJ45 Port
CN7	LAN RJ45 Port
CN8	Touch Screen Lines
CN9	LVDS Control Touch
CN10	NGFF (M-KEY) 2280
CN11	NGFF (E-KEY) 2230
CN12	Power Button (Wafer)
CN13	SPI ROM Flash (Wafer)
CN14	DIO
CN15	COM1 Port
CN16	COM2 Port
CN17	USB2.0 Dual Connector
CN18	USB2.0 Dual Connector
CN19	USB3.2 Gen 2 Dual Port
CN20	USB3.2 Gen 2 Dual Port
CN21	Speaker
CN22	Line Out
CN23	Speaker

Label	Function
CN24	Audio (Wafer)
CN26	Power Input 3P terminal block
CN28	Panel ID
CN29	SATA Power
CN55	COM4 Port (Wafer)
CN61	COM3 Port (Wafer)
JP7	Front Panel
LPC1	Low Pin Count
PCIE1	PCIe Slot
SIM1	SIM card slot
SW1	Power Button

2.4.1 LVDS Port (CN1)

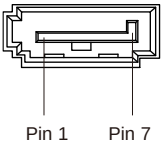
Pin	Signal	Pin	Signal
1	BKL_EN	2	BKL_CTL
3	LVDSVCC	4	GND
5	LVD_A_CLKN	6	LVD_A_CLKP
7	LVDSVCC	8	GND
9	LVD_A_TXN0	10	LVD_A_TXP0
11	LVD_A_TXN1	12	LVD_A_TXP1
13	LVD_A_TXN2	14	LVD_A_TXP2
15	LVD_A_TXN3	16	LVD_A_TXP3
17	LVD_DDC_SDA	18	LVD_DDC_SCL
19	LVD_B_TXN0	20	LVD_B_TXP0
21	LVD_B_TXN1	22	LVD_B_TXP1
23	LVD_B_TXN2	24	LVD_B_TXP2

Pin	Signal	Pin	Signal
25	LVD_B_TXN3	26	LVD_B_TXP3
27	LVDSVCC	28	GND
29	LVD_B_CLKN	30	LVD_B_CLKP

2.4.2 LVDS Inverter (CN2

Pin	Signal	Pin	Signal
1	VDD	2	BKL_CTL
3	GND	4	GND
5	BKL_EN		

2.4.3 SATA Port (CN3)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

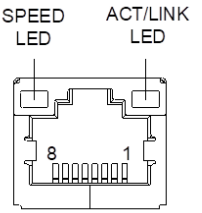
2.4.4 HDMI Port (CN4)

CN4 HDMI Port follows standard specifications.

2.4.5 VGA Port (Wafer Box, Optional)

Pin	Signal	Pin	Signal
1	VSYNC	8	GND
2	HSYNC	9	GREEN
3		10	GND
4	DDC_CLK	11	RED
5	DDC_DAT	12	GND
6	GND	13	5V
7	BLUE		

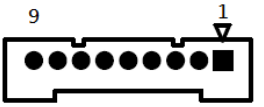
2.4.6 LAN1/LAN2 Port (CN6/CN7)



Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI1-	DIFF	
5	MDI2+	DIFF	

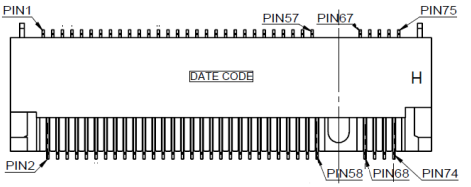
Pin	Pin Name	Signal Type	Signal Level
6	MDI2-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.4.7 Touch Screen Lines (CN8)



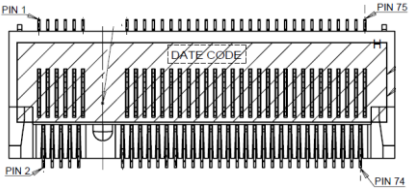
Pin	Signal	Pin	Signal
1	GND	2	TOP EXCITE
3	BOTTOM EXCITE	4	LEFT EXCITE
5	RIGHT EXCITE	6	TOP SENSE
7	BOTTOM SENSE	8	LEFT SENSE
9	RIGHT SENSE		

2.4.8 NGFF (M-Key) 2280 (CN10)



CN10 M.2 M-Key follows standard specifications

2.4.9 NGFF (E-Key) 2230 (CN11)



CN11 M.2 E-Key follows standard specifications

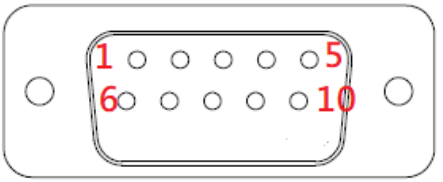
2.4.10 Power Button (Wafer, Reserve) (CN12)

Pin	Pin Name
1	FP_PANSWH#
2	GND

2.4.11 SPI Flash Port (CN13)

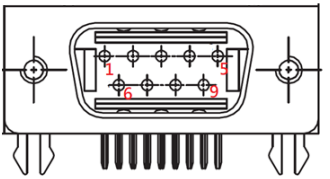
Pin	Pin Name	Signal Type	Signal Level
1	SPI_MISO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_MOSI	IN	
6	SPI_CS	IN	
7	NC		
8	NC		

2.4.12 DIO Port (CN14)



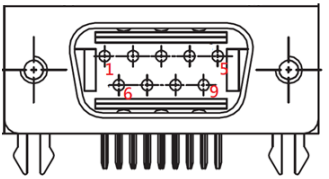
Pin	Pin Name	Signal Type	Signal Level
1	DIO0	I/O	+5V
2	DIO1	I/O	+5V
3	DIO2	I/O	+5V
4	DIO3	I/O	+5V
5	DIO4	I/O	+5V
6	DIO5	I/O	+5V
7	DIO6	I/O	+5V
8	DIO7	I/O	+5V
9	+5V	PWR	+5V
10	GND	GND	

2.4.13 COM1 Port (CN15)



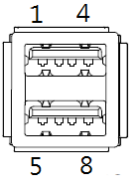
Pin	Pin Name	Signal Type	Signal Level
1	DCD1	IN	
2	RX1	IN	
3	TX1	OUT	±9V
4	DTR1	OUT	±9V
5			
6	DSR1	IN	
7	RTS1	OUT	±9V
8	CTS1	IN	
9	RI1	IN	

2.4.14 COM2 Port (CN16)



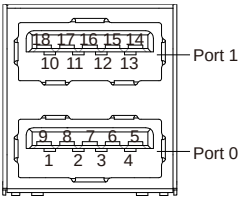
Pin	Pin Name	Signal Type	Signal Level
1	DCD2	IN	
2	RX2	IN	
3	TX2	OUT	±9V
4	DTR2	OUT	±9V
5			
6	DSR2	IN	
7	RTS2	OUT	±9V
8	CTS2	IN	
9	RI2	IN	

2.4.15 USB2.0 Dual Connector (CN17/CN18)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	USBD-	DIFF	
3	USBD+	DIFF	
4	GND	GND	
5	GND	GND	

2.4.16 USB3.2 Gen 2 Connector (CN19/CN20)



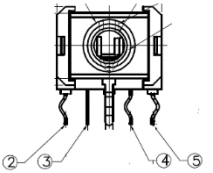
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB1_D-	DIFF	
3	USB1_D+	DIFF	
4	GND	GND	
5	USB1_SSRX–	DIFF	

Pin	Pin Name	Signal Type	Signal Level
6	USB1_SSRX+	DIFF	
7	GND	GND	
8	USB1_SSTX–	DIFF	
9	USB1_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB2_D-	DIFF	
12	USB2_D+	DIFF	
13	GND	GND	
14	USB2_SSRX–	DIFF	
15	USB2_SSRX+	DIFF	
16	GND	GND	
17	USB2_SSTX–	DIFF	
18	USB2_SSTX+	DIFF	

2.4.17 Speaker (CN21)

Pin	Pin Name
1	SPK-L-
2	SPK-L+

2.4.18 Line Out (CN22)

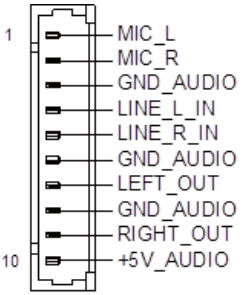


Pin	Pin Name	Pin	Pin Name
1	AUD_GND	2	LOUT_R
3	5V	4	HP_DET
5	LOUT_L		

2.4.19 Speaker (CN23)

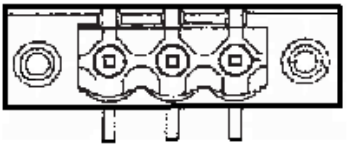
Pin	Pin Name
1	SPK-R-
2	SPK-R+

2.4.20 Audio I/O Port (10P Pitch: 1.25mm) (CN24)



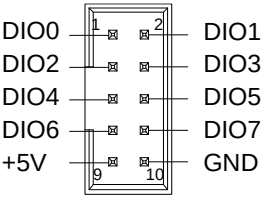
Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LINE_L_IN	IN	
5	LINE_R_IN	IN	
6	GND_AUDIO	GND	
7	LEFT_OUT	OUT	
8	GND_AUDIO	GND	
9	RIGHT_OUT	OUT	
10	+5V_AUDIO	PWR	+5V

2.4.21 Power Input 3-pin Terminal Block (CN26)



Pin	Pin Name	Signal Type	Signal Level
1	VIN	PWR	+10V~+35V
2	GND	GND	
3	GND_EARTH		

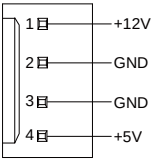
2.4.22 DIO (Panel ID) Port (CN28)



Pin	Pin Name	Signal Type	Signal Level
1	PANEL_ID1	I/O	+5V
2	PANEL_ID2	I/O	+5V
3	PANEL_ID3	I/O	+5V
4	PANEL_ID4	I/O	+5V
5	PANEL_ID5	I/O	+5V
6	PANEL_ID6	I/O	+5V
7	PANEL_ID7	I/O	+5V

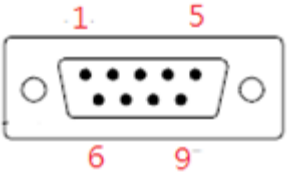
Pin	Pin Name	Signal Type	Signal Level
8	PANEL_ID8	I/O	+5V
9	NC		
10	NC		

2.4.23 SATA Power Connector (CN29)



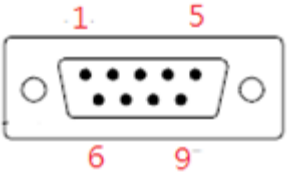
Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	
3	GND	GND	
4	+5V	PWR	+5V

2.4.24 COM4 Port (CN55)



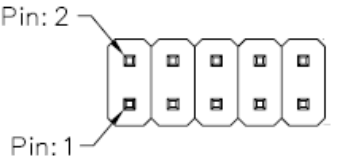
Pin	Pin Name	Signal Type	Signal Level
1	DCD4	IN	
2	RX4	IN	
3	TX4	OUT	±9V
4	DTR4	OUT	±9V
5			
6	DSR4	IN	
7	RTS4	OUT	±9V
8	CTS4	IN	
9	RI4	IN	

2.4.25 COM3 Port (CN61)



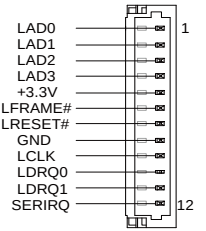
Pin	Pin Name	Signal Type	Signal Level
1	DCD3	IN	
2	RX3	IN	
3	TX3	OUT	±9V
4	DTR3	OUT	±9V
5			
6	DSR3	IN	
7	RTS3	OUT	±9V
8	CTS3	IN	
9	RI3	IN	

2.4.26 Front Panel (JP7)



Pin	Pin Name	Pin	Pin Name
1	GND	2	EXT_PWRBTN#
3	SATA_LED#	4	3.3V
5	FP_SPKR-	6	5V
7	GND	8	PWRLED+
9	GND	10	HWRST#

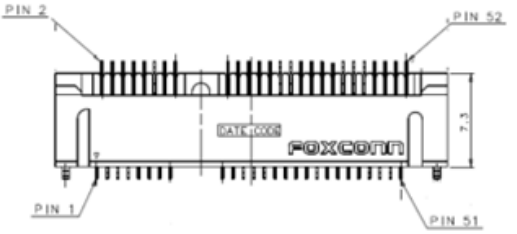
2.4.27 LPC Port (LPC1)



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V

Pin	Pin Name	Signal Type	Signal Level
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.4.28 Mini Card Slot (Full-Sized) (PCIe1)



Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3V	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	NC	PWR	
9	GND	GND	
10	NC	I/O	

Pin	Pin Name	Signal Type	Signal Level
11	PCIE_REF_CLK-	DIFF	
12	NC	IN	
13	PCIE_REF_CLK+	DIFF	
14	NC	IN	
15	GND	GND	
16	NC	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

2.4.29 SIM Slot (SIM1)

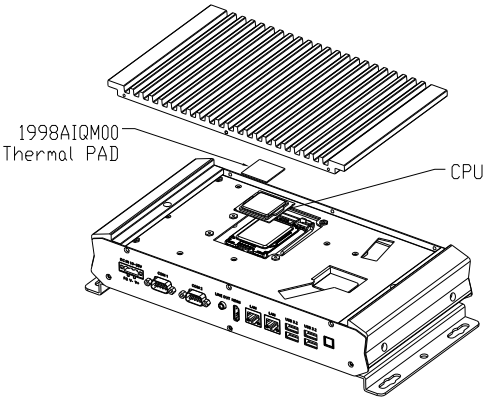
Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	GND	GND	
5	UIM_VPP	PWR	
6	UIM_DATA	I/O	

2.5 CPU Installation

The BOXER-6642-CML utilizes a socket-type CPU configuration, allowing users to easily change or upgrade CPUs within the same socket-type.

Before starting CPU installation, be sure the system is powered down (not in sleep mode) and the power has been disconnected. Also, make sure the CPU is ready for installation.

Step 1: Remove the screws securing the heatsink in place, then set the heatsink aside.



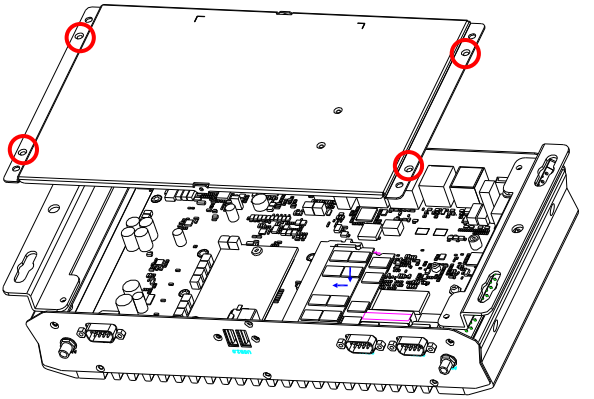
Step 2: Place the CPU into the CPU socket. Then, place the thermal pad on the CPU.

Step 3: Replace the heatsink and secure with the screws you removed in Step 1.

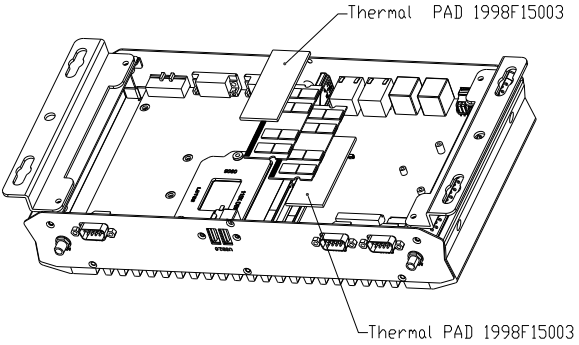
2.6 RAM and 2.5″ Storage Drive installation

Before starting RAM and Storage Drive installation, be sure the system is powered down (not in sleep mode) and the power has been disconnected. Also, make sure the components are ready for installation. For specifications and requirement of memory and storage devices, see Chapter 1: Specifications.

Step 1: Remove the four screws securing the bottom panel, then lift the bottom panel off the device. If you have previously installed a storage device, be careful to disconnect the SATA and SATA power cables before completely removing the bottom panel.



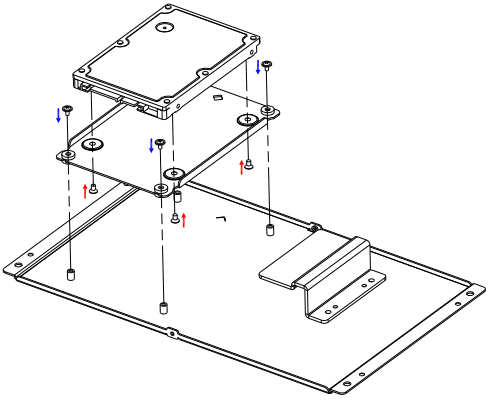
Step 2: Attach a thermal pad to the first RAM module, between the board and module. Then, insert the module at a roughly 30° angle. Gently push down until secured by the tabs.



Step 3: Install the next RAM module, again first by inserting at a 30° angle, then gently pressing down until secured.

Step 4: Place a thermal pad on top of this module. If you are not installing a new storage device, you may proceed to reconnecting and replacing the bottom panel.

Step 5: Attach the 2.5" SATA drive to the drive bracket using four screws supplied.



Step 6: Next, attach the drive bracket to the bottom panel by lining up with the risers as shown in the diagram.

Step 7: Attach the SATA Power and SATA cables to the 2.5" SATA drive.

Step 8: Reattach the bottom panel to the system, in reverse order of Step 1.

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The system configuration was reset by the Clear CMOS jumper
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <ESC> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Chipset – For hosting bridge parameters

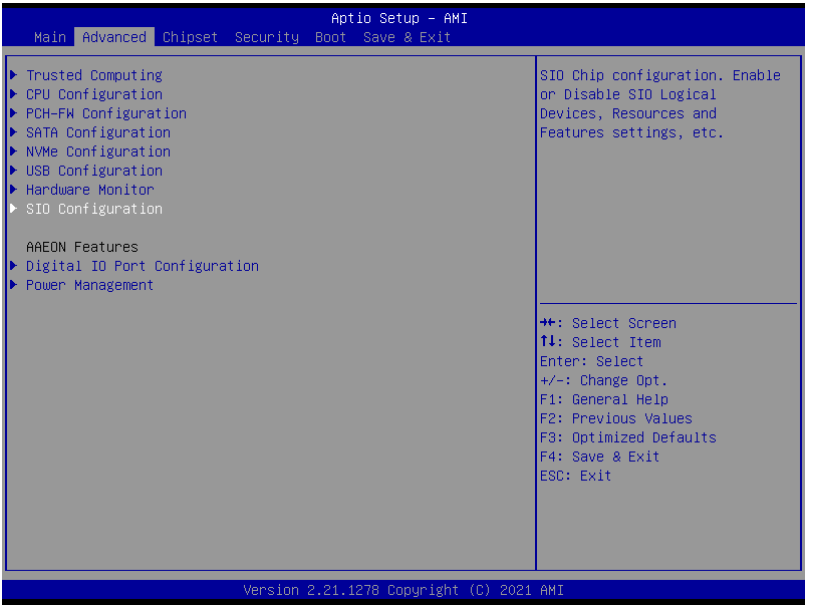
Security – The setup administrator password can be set here

Boot – Enable/ Disable quiet Boot Option

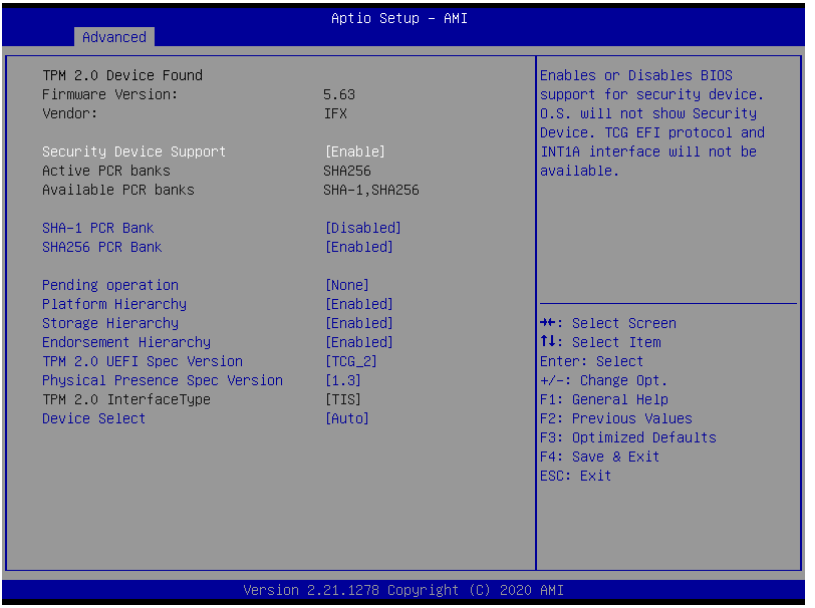
Save & Exit –Save your changes and exit the program

3.3 Setup Submenu: Main

3.4 Setup Submenu: Advanced



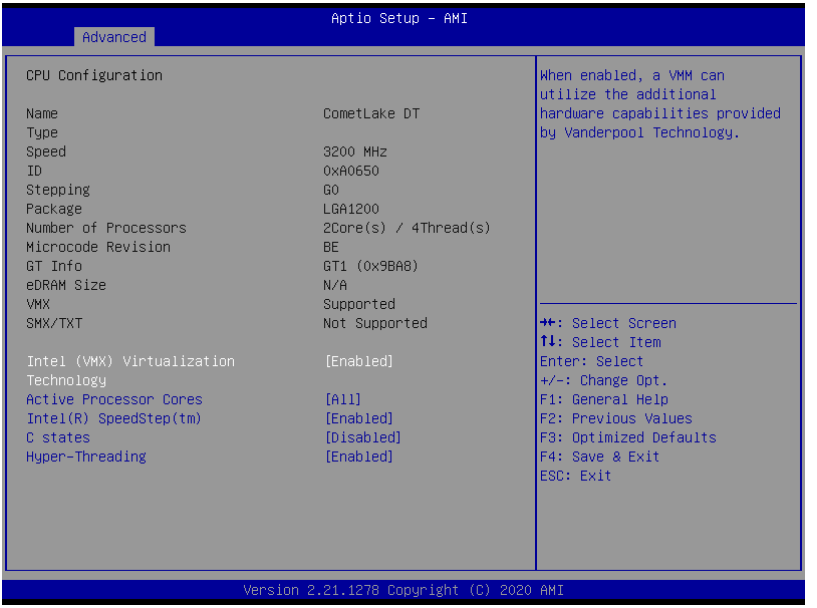
3.4.1 Trusted Computing



Options Summary		
Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable SHA-1 PCR Bank.		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-256 PCR Bank.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change state of Security Device.		
Platform Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Platform Hierarchy		

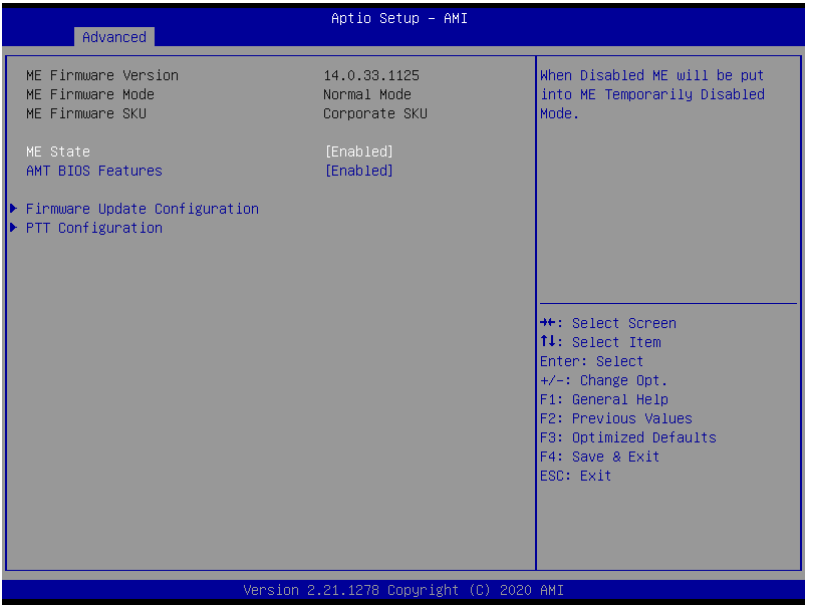
Options Summary		
Storage Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: The Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later.		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 device, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 device will be enumerated.		

3.4.2 CPU Configuration



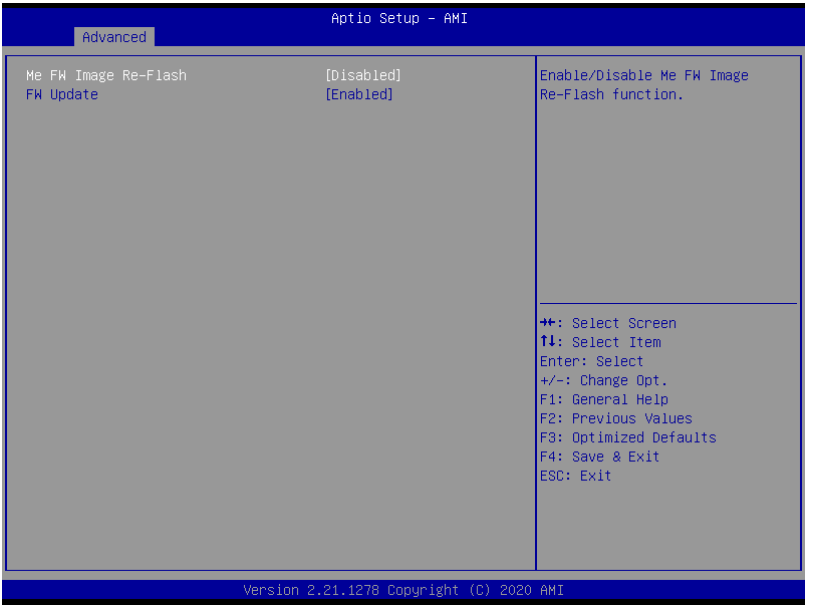
Options Summary		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Active Processor Cores	All	Optimal Default, Failsafe Default
	1	
Number of cores to enable in each processor package.		
Intel® SpeedStep™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
C states	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.		
Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Hyper-Threading Technology.		

3.4.3 PCH-FW Configuration



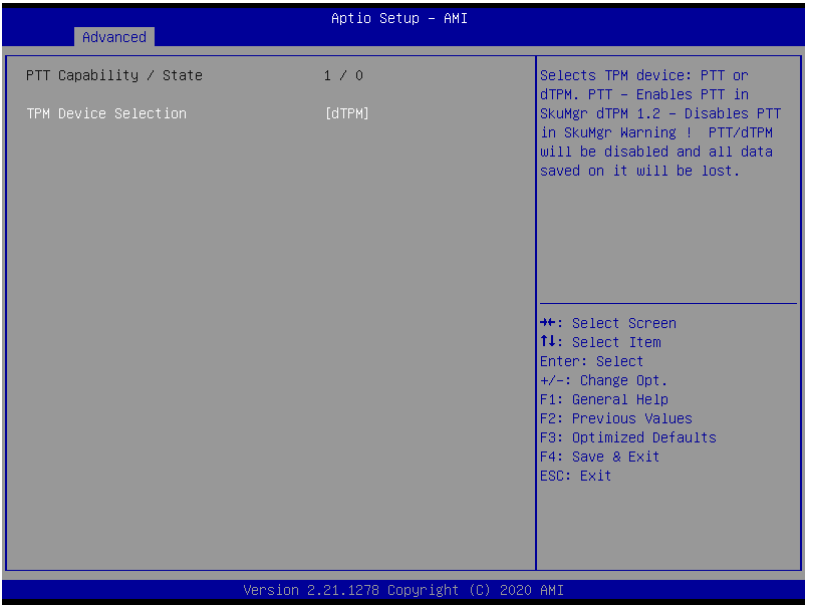
Options Summary		
ME State	Disabled	
	Enabled	Optimal Default, Failsafe Default
When Disabled ME will be put into ME Temporarily Disabled Mode.		
AMT BIOS Features	Disabled	
	Enabled	Optimal Default, Failsafe Default
When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup. Note: This option does not disable Manageability Features in FW.		

3.4.3.1 Firmware Update Configuration



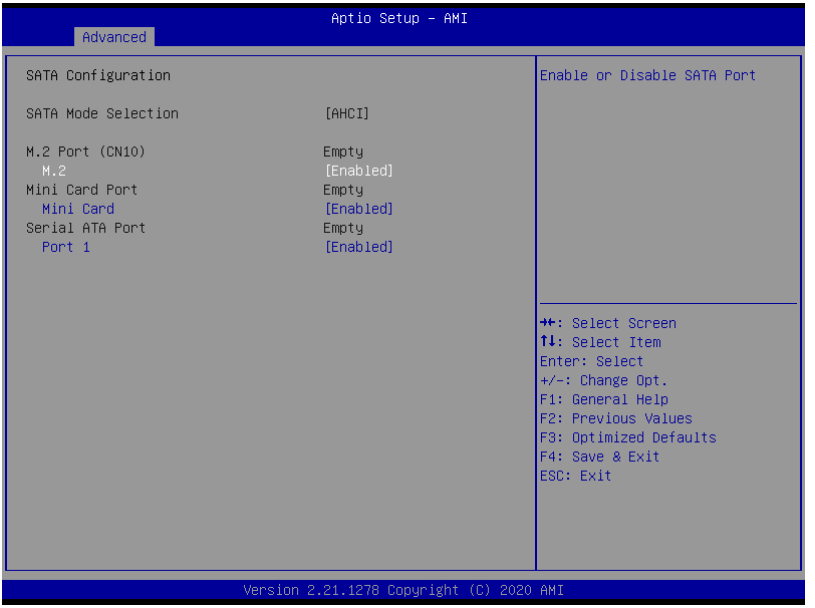
Options Summary		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable ME FW Image Re-Flash function.		
FW Update	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable ME FW Update function.		

3.4.3.2 PTT Configuration



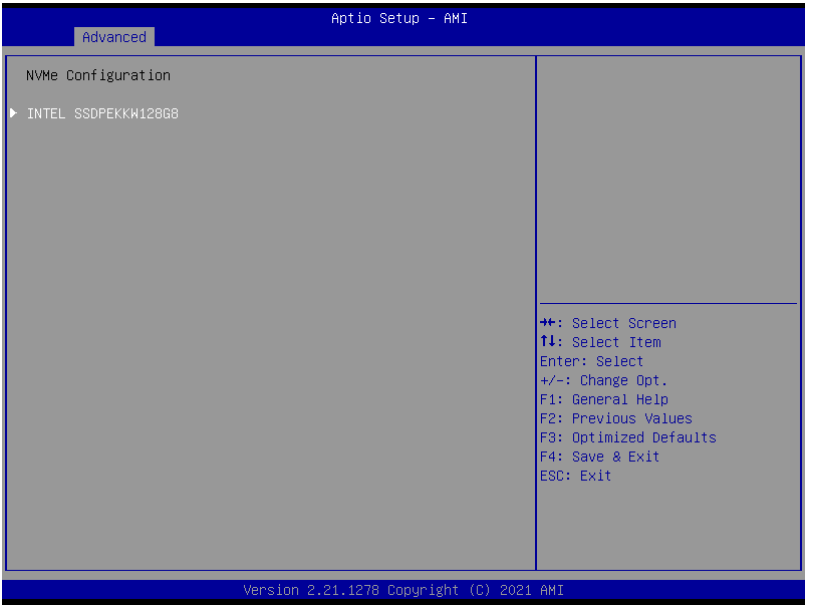
Options Summary		
TPM Device Selection	dTPM	Optimal Default, Failsafe Default
	PTT	
Selects TPM device: PTT or dTPM. PTT – Enables in SkuMgr dTPM 1.2 – Disables PTT in SkuMgr Warning! PTT/dTPM will be disabled and all data saved on it will be lost.		

3.4.4 SATA Configuration



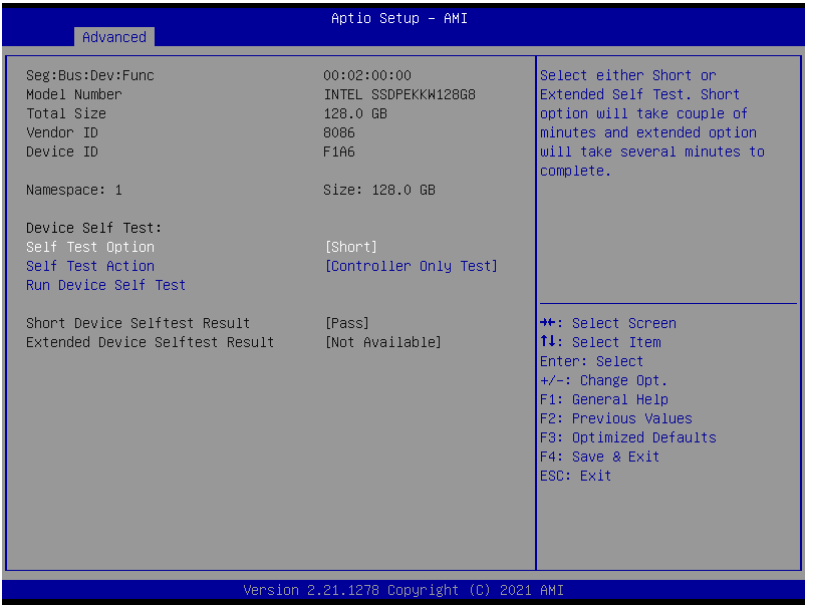
Options Summary		
M.2	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		
Mini Card	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		
Port	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		

3.4.5 NVMe Configuration



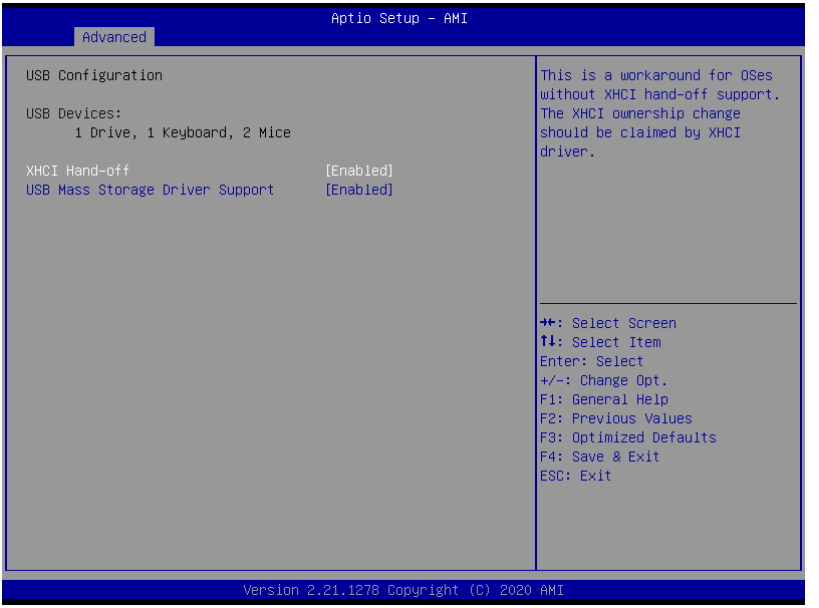
Choose the device to be configured.

3.4.5.1 NVMe Configuration: Device



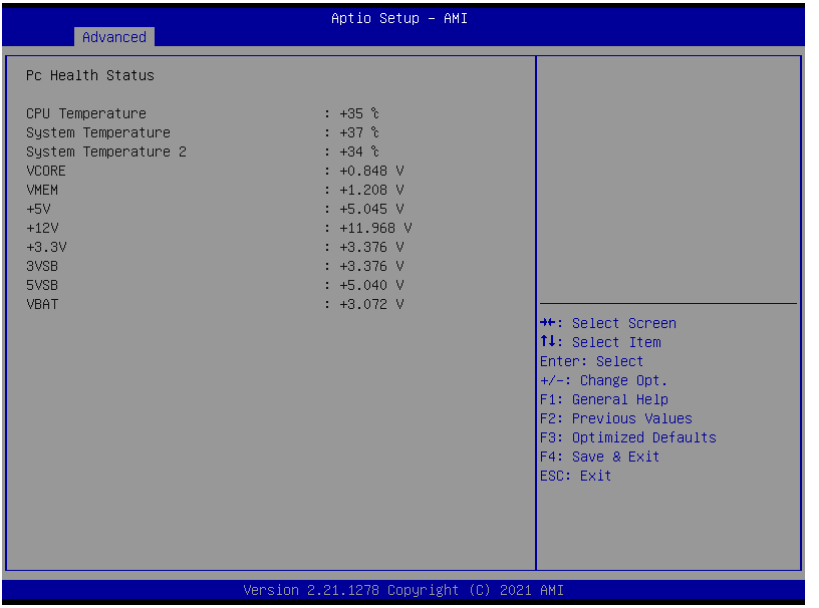
Options Summary		
Self Test Option	Short	Optimal Default, Failsafe Default
	Extended	
Select either Short or Extended Self Test. Short option will take couple of minutes and extended option will take several minutes to complete.		
Self Test Action	Controller Only Test	Optimal Default, Failsafe Default
	Controller and NameSpace Test	
Select either to test Controller alone or Controller and NameSpace. Selecting Controller and Namespace option will take lot longer to complete the test.		
Run Device Self Test		
Perform device self test for the corresponding Option and Action selected by user. Pressing 'Esc' key will abort the test. Result shown below is the recent result logged in the device.		

3.4.6 USB Configuration



Options Summary		
XHCI Hand-off	Disabled	
	Enabled	Optimal Default, Failsafe Default
This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.		
USB Mass Storage Driver Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable USB Mass Storage Driver Support.		

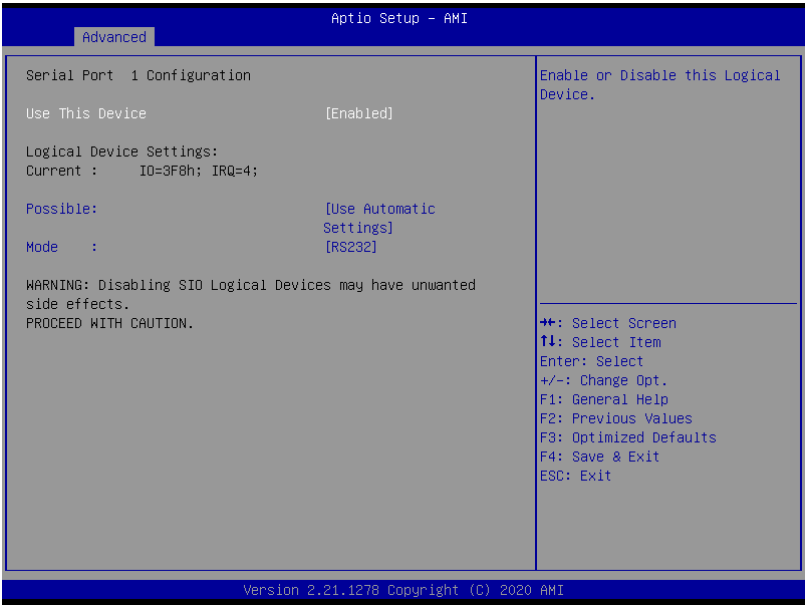
3.4.7 Hardware Monitor



3.4.8 SIO Configuration

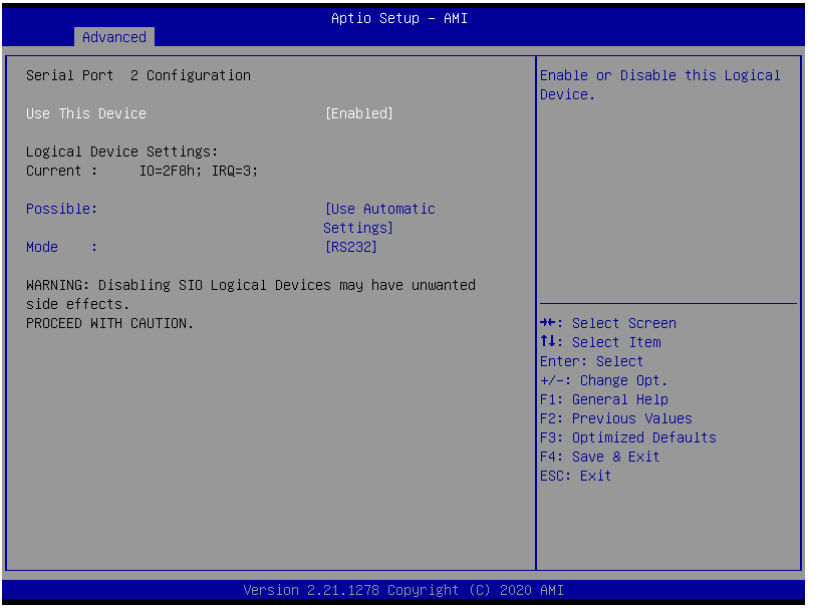
Options Summary		
[*Active*] Serial Port N		
View and Set Basic properties of the SIO Logical device. Like IO Base, IRQ Range, DMA Channel and Device Mode.		

3.4.8.1 SIO Configuration: Serial Port 1



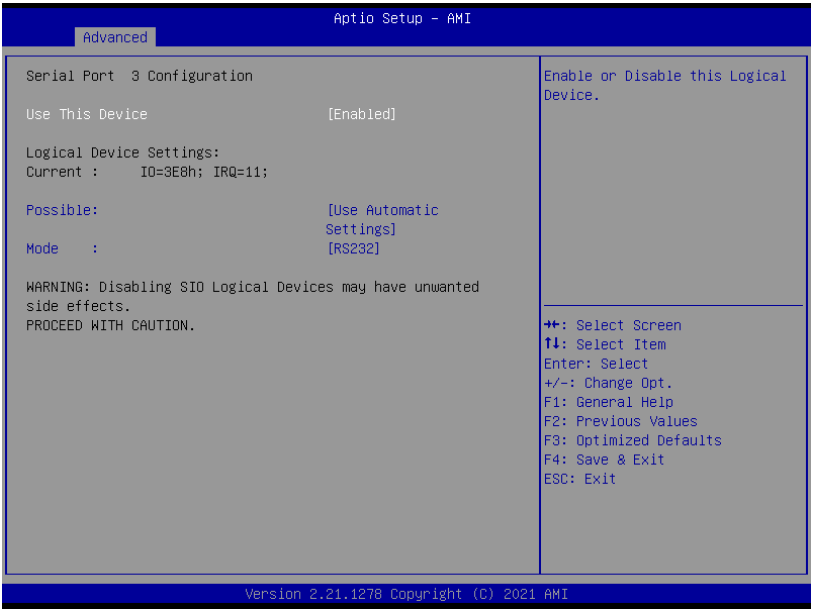
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4;	
	IO=2F8h; IRQ=3;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422 ,485 selection		

3.4.8.2 SIO Configuration: Serial Port 2



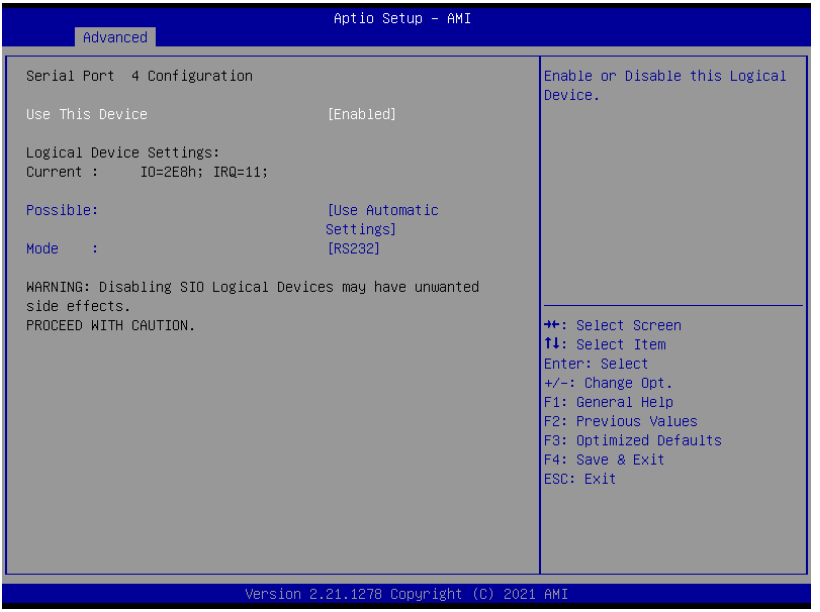
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=4;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422 ,485 selection		

3.4.8.3 SIO Configuration: Serial Port 3



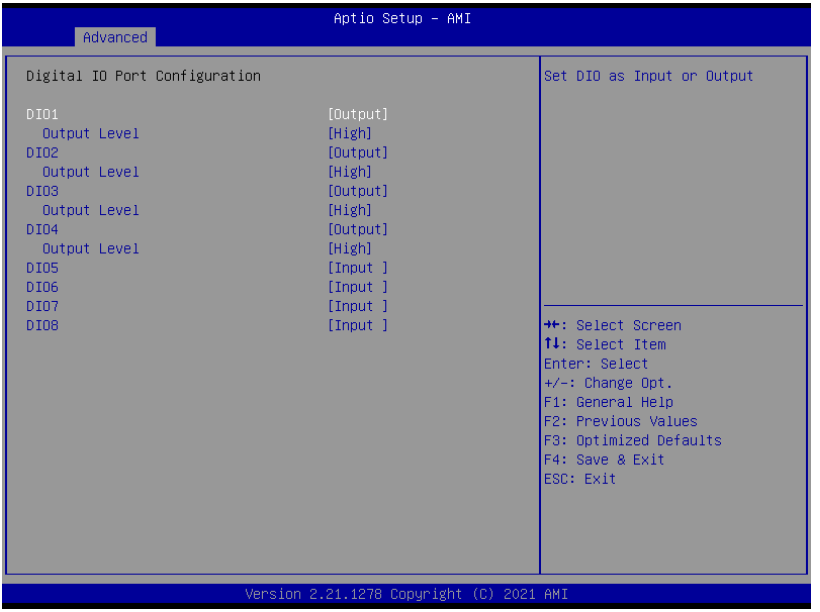
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8h; IRQ=11;	
	IO=2E8h; IRQ=11;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422 ,485 selection		

3.4.8.4 SIO Configuration: Serial Port 4



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2E8h; IRQ=11;	
	IO=3E8h; IRQ=11;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422 ,485 selection		

3.4.9 Digital IO Port Configuration



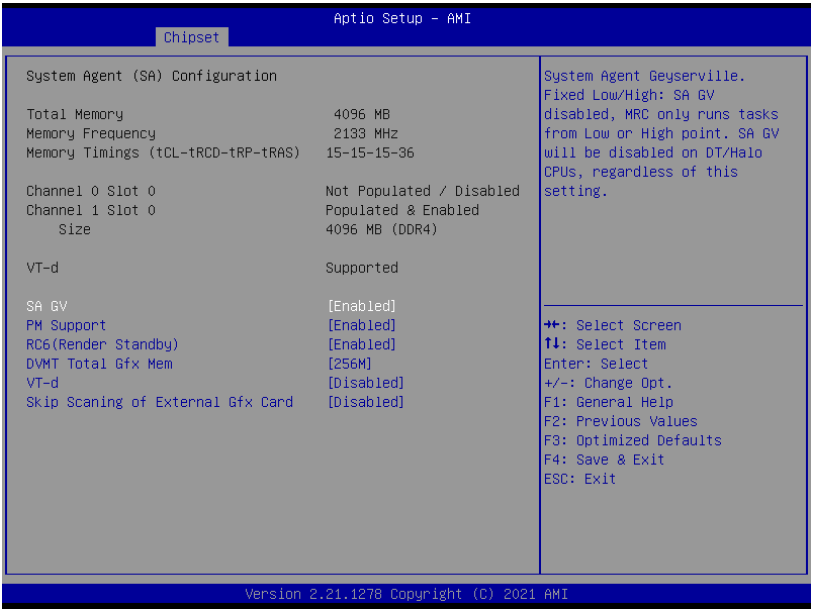
Options Summary		
DIO1/2/3/4/5/6/7/8	Input	
	Output	Optimal Default, Failsafe Default
Set DOP as Input or Output		
Output Level	Low	Optimal Default, Failsafe Default
	High	
Set output level when DIO pin is output		

3.4.9 Power Management

Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
	Bypass	
Fixed Time: System will wake on the hr :: min :: sec specified. Dynamic Time: System will wake on the current time + Increase minutes(s). Bypass: BIOS will not control RTC wake function during system shutdown.		

3.5 Setup Submenu: Chipset

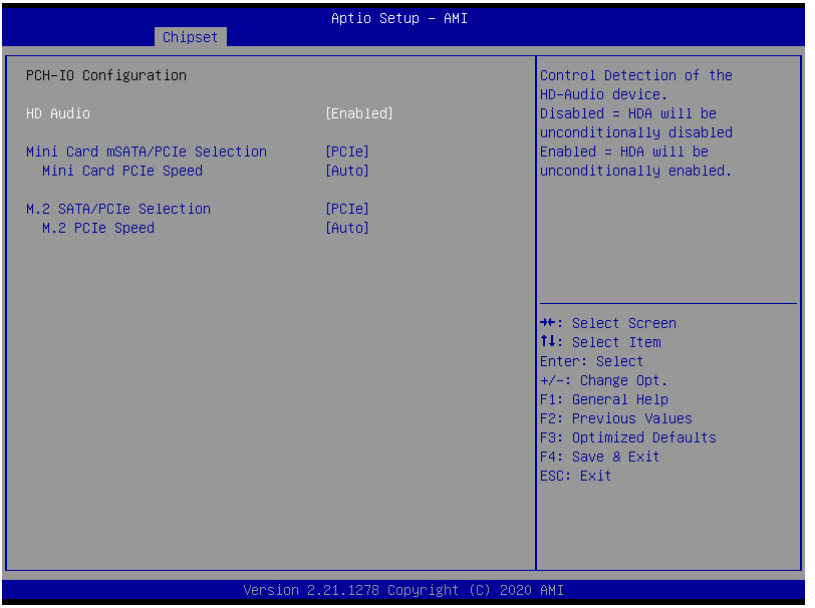
3.5.1 System Agent (SA) Configuration



Options Summary		
SA GV	Disabled	
	Fixed Low	
	Fixed High	
	Enabled	Optimal Default, Failsafe Default
System Agent Geyserville. Fixed Low/High: SA GV disabled, MRC only runs tasks from Low or High point. SA GV will be disabled on DT/Halo CPUs, regardless of this setting.		
PM Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable PM Support		
RC6(Render Standby)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Check to enable render standby support.		
DVMT Total Gfx Mem	128M	
	256M	Optimal Default, Failsafe Default
	MAX	
Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.		

Options Summary		
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
VT-d capability		
Skip Scanning of External Gfx Card	Disabled	Optimal Default, Failsafe Default
	Enabled	
If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports.		

3.5.2 PCH-IO Configuration

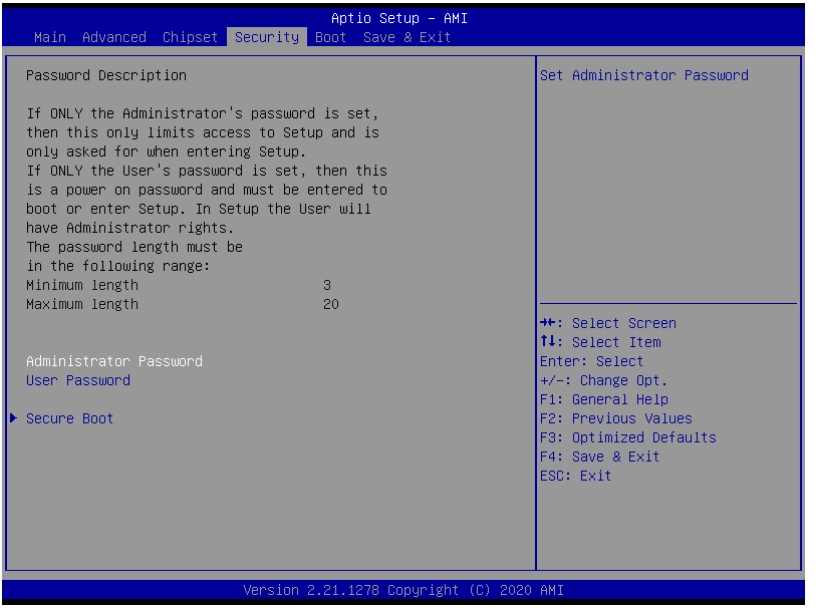


Options Summary		
HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.		
Mini Card mSATA/PCIe Selection	PCIe	Optimal Default, Failsafe Default
	mSATA	
Select mSATA or PCIe function for Mini-Card.		
Mini Card PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed.		
M.2 SATA/PCIe Selection	PCIe	Optimal Default, Failsafe Default
	SATA	
Select SATA or PCIe function for M.2		

Table Continues on Next Page...

Options Summary		
M.2 PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed.		

3.6 Setup Submenu: Security



Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

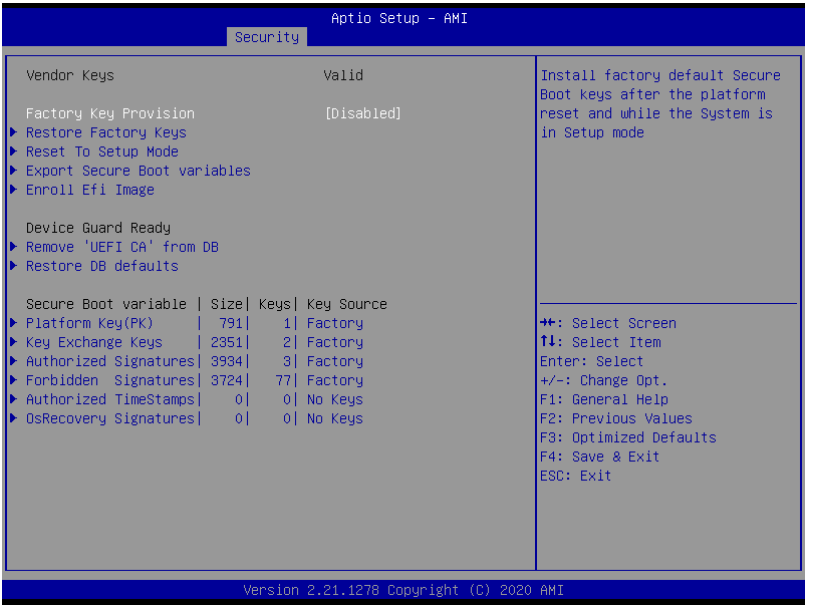
Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Secure Boot

Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Standard	
	Custom	Optimal Default, Failsafe Default
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys	Force system to user mode. Install factory default Secure Boot key databases.	
Reset to Setup Mode	Delete all Secure Boot key databases from NVRAM.	

3.6.1.1 Key Management



Options Summary		
Provision Factory Defaults	Disabled	Optimal Default, Failsafe Default
	Enabled	
Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.		
Restore Factory Keys	Force system to user mode. Install factory default Secure Boot key databases.	
Reset to Setup Mode	Delete all Secure Boot key databases from NVRAM.	
Export Secure Boot Variables	Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device	
Enroll EFI Image	Allow the image to run in Secure Boot mode. Enroll SHA256 hash of a PE image into Authorized Signature Database (db).	
Remove 'UEFI CA' from DB	Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)	
Restore DB defaults	Restore DB variable to factory defaults.	
Save all Secure Boot Variables.	Save NVRAM content of Secure Boot policy variables to the files (EFI_SIGNATURE_LIST data format) in root folder on a target file system device.	

Secure Boot Variables

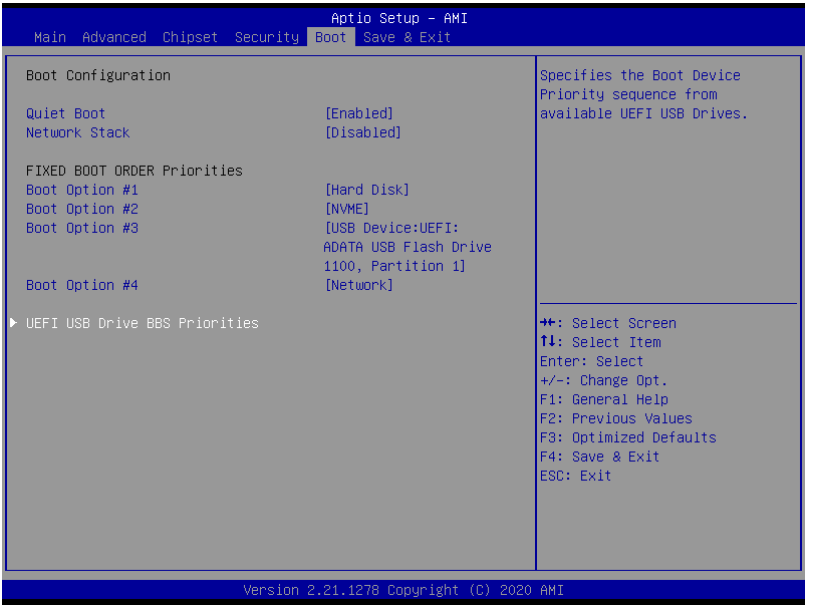
Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:
   a) EFI_SIGNATURE_LIST
   b) EFI_CERT_X509 (DER encoded)
   c) EFI_CERT_RSA2048 (bin)
   d) EFI_CERT_SHA256,384,512
2. Authenticated UEFI Variable
3. EFI PE/COFF Image (SHA256)

Key Source:

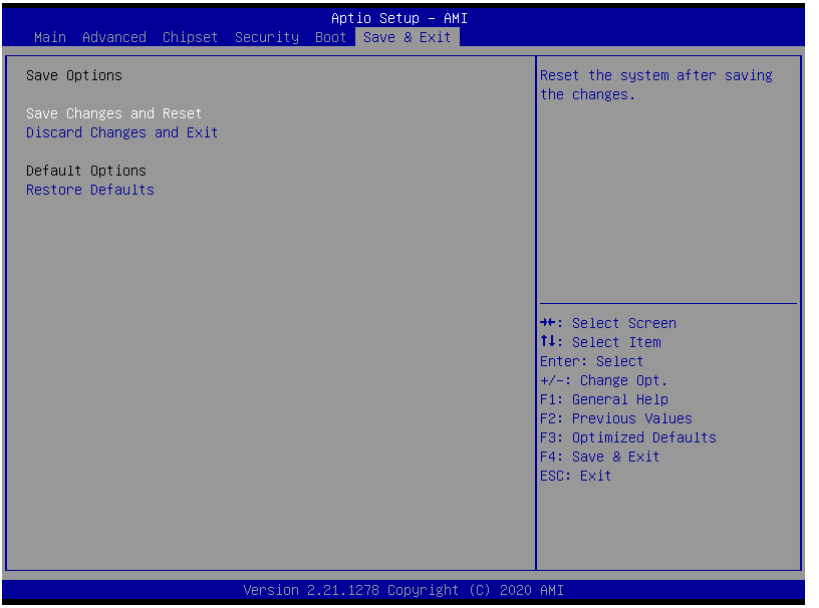
Default, External, Mixed, Test

3.7 Setup Submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Quiet Boot option.		
Network Stack	Enabled	
	Disabled	Optimal Default, Failsafe Default
Enable/Disable UEFI Network Stack.		
FIXED BOOT ORDER Priorities	Sets the system boot order.	

3.8 Setup Submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Drivers Download and Installation

Drivers for the BOXER-6642-CML can be downloaded from the product page on the AAEON website by following this link:

[add link once website is ready]

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Drivers

1. Open the **Step 1 – Chipset** folder and select your OS
2. Open the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphics Drivers

1. Open the **Step 2 - Graphic** folder and select your OS
2. Open the **igxpin.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install LAN Drivers

1. Open the **Step 3 – LAN** folder and select your OS
2. Open the **PROWinx64.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install USB3.0 Drivers (Windows 7 Only)

1. Open the **Step 4 – USB3.0** folder and open the Win 7 folder
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install Serial Port Drivers (Optional)

1. Open the **Step 5 –Serial Port Driver (Optional)** folder
2. Open the **FintekSerial.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1: SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2: Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0xF5(Note6)	3(Note7)	0(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07(Note9)	0xF5(Note10)	5(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0xF5(Note14)	6(Note15)	1	1: Clear timeout status
Output Mode	0x07(Note16)	0xF5(Note17)	4(Note18)	1(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07(Note20)	0xFA(Note21)	0(Note22)	1(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```
**********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte    SIOIndex    //This parameter is represented from Note1
#define byte    SIOData    //This parameter is represented from Note2
#define    void    IOWriteByte(byte IOPort, byte Value);
#define    byte    IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte    TimerLDN    //This parameter is represented from Note3
#define byte    TimerReg    //This parameter is represented from Note4
#define byte    TimerVal    // This parameter is represented from Note24
#define byte    UnitLDN    //This parameter is represented from Note5
#define byte    UnitReg    //This parameter is represented from Note6
#define byte    UnitBit    //This parameter is represented from Note7
#define byte    UnitVal    //This parameter is represented from Note8
#define byte    EnableLDN    //This parameter is represented from Note9
#define byte    EnableReg    //This parameter is represented from Note10
#define byte    EnableBit    //This parameter is represented from Note11
#define byte    EnableVal    //This parameter is represented from Note12
#define byte    StatusLDN    // This parameter is represented from Note13
#define byte    StatusReg    // This parameter is represented from Note14
#define byte    StatusBit    // This parameter is represented from Note15
#define byte    ModeLDN    // This parameter is represented from Note16
#define byte    ModeReg    // This parameter is represented from Note17
#define byte    ModeBit    // This parameter is represented from Note18
#define byte    ModeVal    // This parameter is represented from Note19
#define byte    WDTRstLDN    // This parameter is represented from Note20
#define byte    WDTRstReg    // This parameter is represented from Note21
#define byte    WDTRstBit    // This parameter is represented from Note22
#define byte    WDTRstVal    // This parameter is represented from Note23
**********************************************************************************
```

```
*******************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Time of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig();

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*******************************************************************************
```

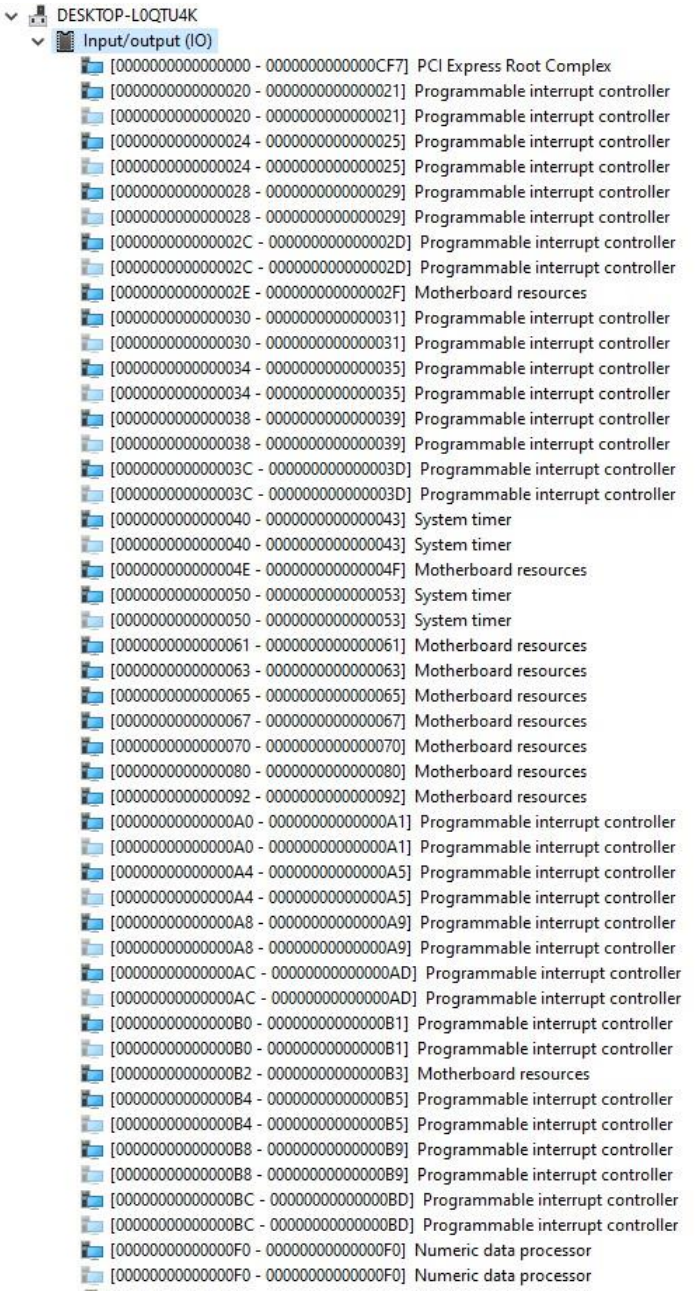
```
**********************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (){
         // Disable WDT counting
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
         // Clear Watchdog Timeout Status
         WDTClearTimeoutStatus();
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID   WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
        SIOBitSet(LDN, Register, BitNum, Value);
}

VOID   WDTParameterSetting(){
         // Watchdog Timer counter setting
         SIOByteSet(TimerLDN, TimerReg, TimerVal);
        // WDT counting unit setting
        SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
        // WDT output mode setting, level / pulse
        SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
         // Watchdog timeout output via WDTRST#
         SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID   WDTClearTimeoutStatus(){
        SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
**********************************************************************************
```

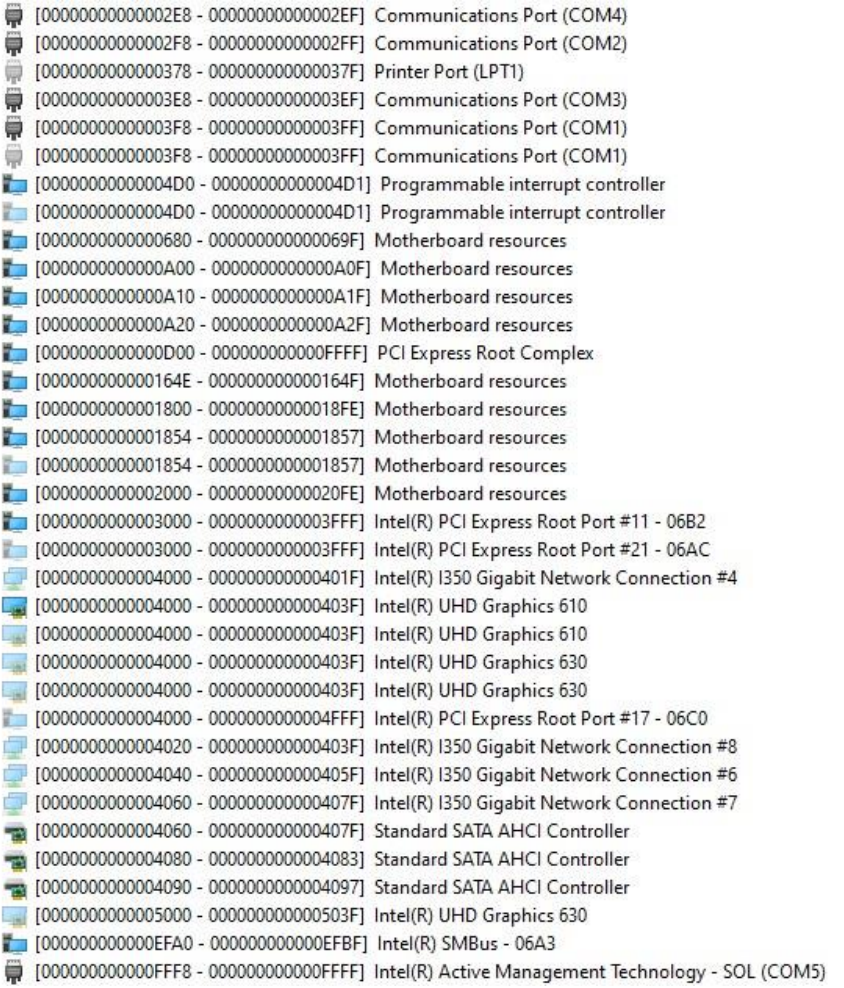
```
*********************************************************************************
VOID   SIOEnterMBPnPMode(){
       IOWriteByte(SIOIndex, 0x87);
       IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*********************************************************************************
```

Appendix B

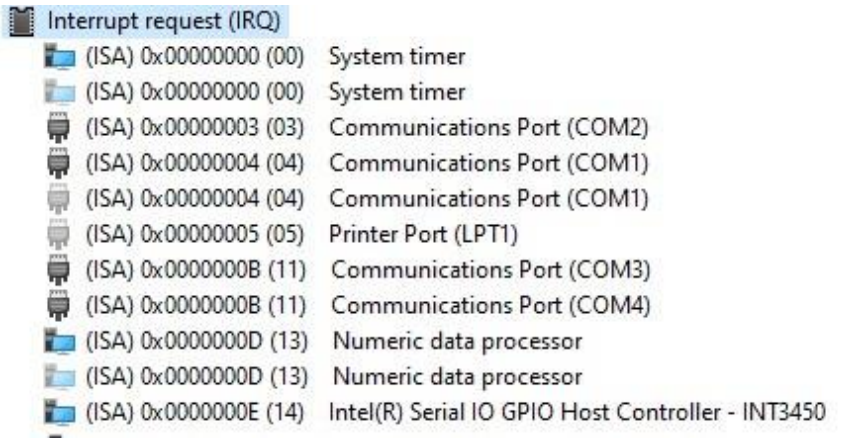
I/O Information

B.1 I/O Address Map

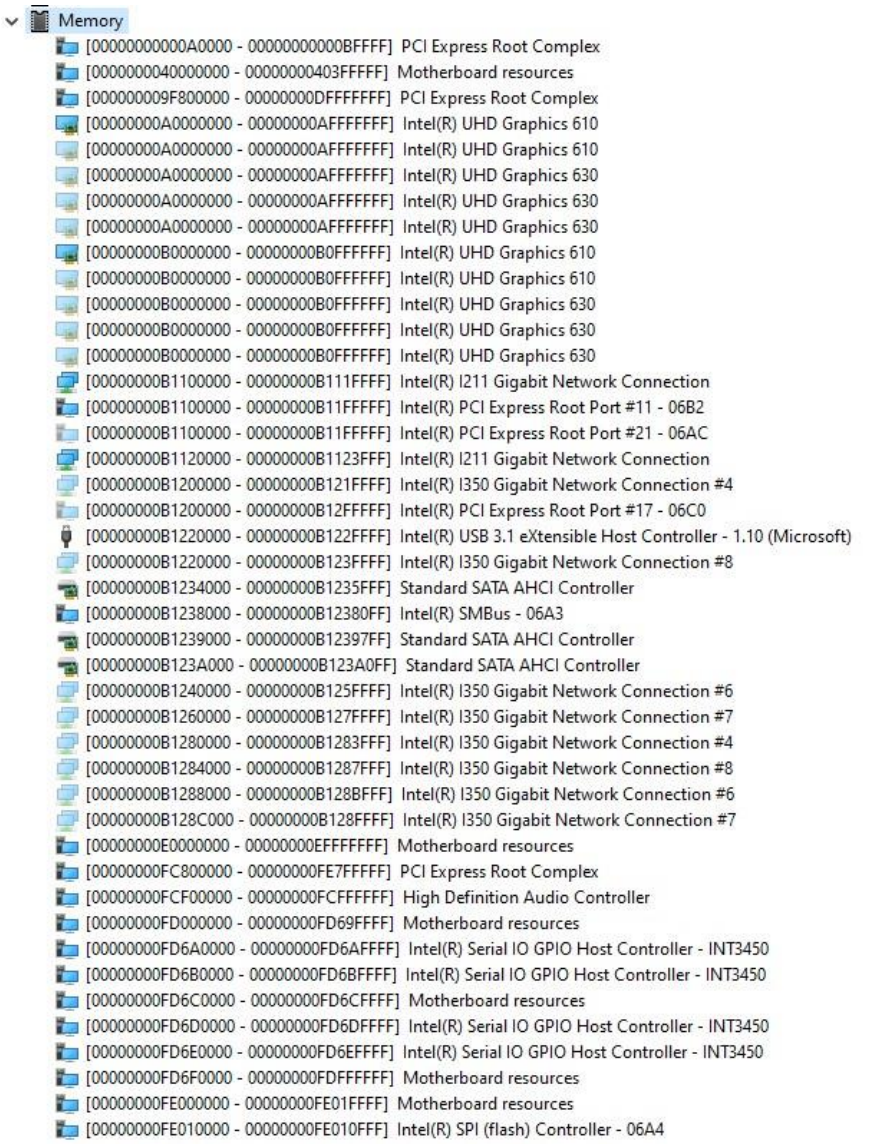


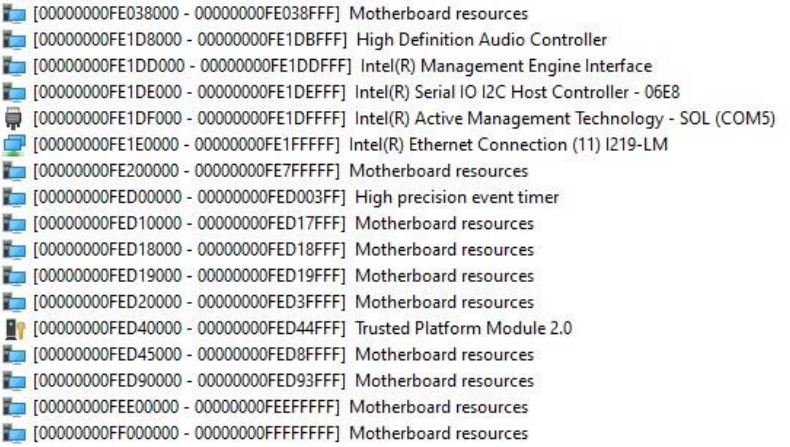

[00000000000002E8 - 00000000000002EF] Communications Port (COM4)
[00000000000002F8 - 00000000000002FF] Communications Port (COM2)
[0000000000000378 - 000000000000037F] Printer Port (LPT1)
[00000000000003E8 - 00000000000003EF] Communications Port (COM3)
[00000000000003F8 - 00000000000003FF] Communications Port (COM1)
[00000000000003F8 - 00000000000003FF] Communications Port (COM1)
[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
[0000000000000680 - 000000000000069F] Motherboard resources
[0000000000000A00 - 0000000000000A0F] Motherboard resources
[0000000000000A10 - 0000000000000A1F] Motherboard resources
[0000000000000A20 - 0000000000000A2F] Motherboard resources
[0000000000000D00 - 000000000000FFFF] PCI Express Root Complex
[000000000000164E - 000000000000164F] Motherboard resources
[0000000000001800 - 00000000000018FE] Motherboard resources
[0000000000001854 - 0000000000001857] Motherboard resources
[0000000000001854 - 0000000000001857] Motherboard resources
[0000000000002000 - 00000000000020FE] Motherboard resources
[0000000000003000 - 0000000000003FFF] Intel(R) PCI Express Root Port #11 - 06B2
[0000000000003000 - 0000000000003FFF] Intel(R) PCI Express Root Port #21 - 06AC
[0000000000004000 - 000000000000401F] Intel(R) I350 Gigabit Network Connection #4
[0000000000004000 - 000000000000403F] Intel(R) UHD Graphics 610
[0000000000004000 - 000000000000403F] Intel(R) UHD Graphics 610
[0000000000004000 - 000000000000403F] Intel(R) UHD Graphics 630
[0000000000004000 - 000000000000403F] Intel(R) UHD Graphics 630
[0000000000004000 - 0000000000004FFF] Intel(R) PCI Express Root Port #17 - 06C0
[0000000000004020 - 000000000000403F] Intel(R) I350 Gigabit Network Connection #8
[0000000000004040 - 000000000000405F] Intel(R) I350 Gigabit Network Connection #6
[0000000000004060 - 000000000000407F] Intel(R) I350 Gigabit Network Connection #7
[0000000000004060 - 000000000000407F] Standard SATA AHCI Controller
[0000000000004080 - 0000000000004083] Standard SATA AHCI Controller
[0000000000004090 - 0000000000004097] Standard SATA AHCI Controller
[0000000000005000 - 000000000000503F] Intel(R) UHD Graphics 630
[000000000000EFA0 - 000000000000EFBF] Intel(R) SMBus - 06A3
[000000000000FFF8 - 000000000000FFFF] Intel(R) Active Management Technology - SOL (COM5)

B.2 IRQ Mapping Chart



B.3 Memory Address Map

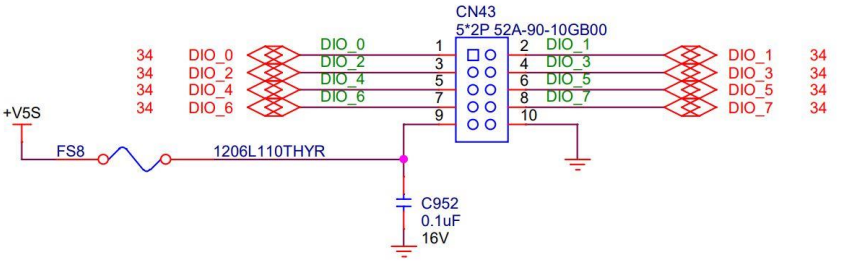



[00000000FE038000 - 00000000FE038FFF] Motherboard resources
[00000000FE1D8000 - 00000000FE1DBFFF] High Definition Audio Controller
[00000000FE1DD000 - 00000000FE1DDFFF] Intel(R) Management Engine Interface
[00000000FE1DE000 - 00000000FE1DEFFF] Intel(R) Serial IO I2C Host Controller - 06E8
[00000000FE1DF000 - 00000000FE1DFFFF] Intel(R) Active Management Technology - SOL (COM5)
[00000000FE1E0000 - 00000000FE1FFFFF] Intel(R) Ethernet Connection (11) I219-LM
[00000000FE200000 - 00000000FE7FFFFF] Motherboard resources
[00000000FED00000 - 00000000FED003FF] High precision event timer
[00000000FED10000 - 00000000FED17FFF] Motherboard resources
[00000000FED18000 - 00000000FED18FFF] Motherboard resources
[00000000FED19000 - 00000000FED19FFF] Motherboard resources
[00000000FED20000 - 00000000FED3FFFF] Motherboard resources
[00000000FED40000 - 00000000FED44FFF] Trusted Platform Module 2.0
[00000000FED45000 - 00000000FED8FFFF] Motherboard resources
[00000000FED90000 - 00000000FED93FFF] Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources
[00000000FF000000 - 00000000FFFFFFFF] Motherboard resources

Appendix C

Digital I/O Ports

C.1 Electrical Specifications for Digital I/O Ports



GPIO70	DIO_0
GPIO71	DIO_1
GPIO72	DIO_2
GPIO73	DIO_3
GPIO74	DIO_4
GPIO75	DIO_5
GPIO76	DIO_6
GPIO77	DIO_7

C.2 DIO Programming

BOXER-6642-CML utilizes FINTEK F81966 chipset as its Digital I/O controller. The following sections detail the procedures to complete its configuration. The AAEON initial DIO program is also attached to help with developing a customized program for your application.

There are three steps to complete the configuration setup:

Step 1 Enter MB PnP Mode.

Step 2 Modify the data in the configuration registers.

Step 3 Exit MB PnP Mode. Undesired results may occur if MB PnP Mode is not exited properly.

C.2 Digital I/O Register

Table 1: SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2: Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0x82(Note4)	0(Note5)		GPIO70
DIO-2 Pin Status	0x06(Note6)	0x82(Note7)	1(Note8)		GPIO71
DIO-3 Pin Status	0x06(Note9)	0x82(Note10)	2(Note11)		GPIO72
DIO-4 Pin Status	0x06(Note12)	0x82(Note13)	3(Note14)		GPIO73
DIO-5 Pin Status	0x06(Note15)	0x82(Note16)	4(Note17)		GPIO74
DIO-6 Pin Status	0x06(Note18)	0x82(Note19)	5(Note20)		GPIO75
DIO-7 Pin Status	0x06(Note21)	0x82(Note22)	6(Note23)		GPIO76
DIO-8 Pin Status	0x06(Note24)	0x82(Note25)	7(Note26)		GPIO77

Table 3: Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0x81(Note28)	0(Note29)	(Note30)	GPIO70
DIO-2 Output Data	0x06(Note31)	081(Note32)	1(Note33)	(Note34)	GPIO71
DIO-3 Output Data	0x06(Note35)	0x81(Note36)	2(Note37)	(Note38)	GPIO72
DIO-4 Output Data	0x06(Note39)	0x81(Note40)	3(Note41)	(Note42)	GPIO73
DIO-5 Output Data	0x06(Note43)	0x81(Note44)	4(Note45)	(Note46)	GPIO74
DIO-6 Output Data	0x06(Note47)	0x81(Note48)	5(Note49)	(Note50)	GPIO75
DIO-7 Output Data	0x06(Note51)	0x81(Note52)	6(Note53)	(Note54)	GPIO76
DIO-8 Output Data	0x06(Note55)	0x81(Note56)	7(Note57)	(Note58)	GPIO77

C.3 Digital I/O Sample Program

```
**********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define  void   IOWriteByte(byte IOPort, byte Value);
#define  byte   IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DInput1LDN   // This parameter is represented from Note3
#define byte   DInput1Reg   // This parameter is represented from Note4
#define byte   DInput1Bit   // This parameter is represented from Note5
#define byte   DInput2LDN   // This parameter is represented from Note6
#define byte   DInput2Reg   // This parameter is represented from Note7
#define byte   DInput2Bit   // This parameter is represented from Note8
#define byte   DInput3LDN   // This parameter is represented from Note9
#define byte   DInput3Reg   // This parameter is represented from Note10
#define byte   DInput3Bit   // This parameter is represented from Note11
#define byte   DInput4LDN   // This parameter is represented from Note12
#define byte   DInput4Reg   // This parameter is represented from Note13
#define byte   DInput4Bit   // This parameter is represented from Note14
#define byte   DInput5LDN   // This parameter is represented from Note15
#define byte   DInput5Reg   // This parameter is represented from Note16
#define byte   DInput5Bit   // This parameter is represented from Note17
#define byte   DInput6LDN   // This parameter is represented from Note18
#define byte   DInput6Reg   // This parameter is represented from Note19
#define byte   DInput6Bit   // This parameter is represented from Note20
#define byte   DInput7LDN   // This parameter is represented from Note21
#define byte   DInput7Reg   // This parameter is represented from Note22
#define byte   DInput7Bit   // This parameter is represented from Note23
#define byte   DInput8LDN   // This parameter is represented from Note24
#define byte   DInput8Reg   // This parameter is represented from Note25
#define byte   DInput8Bit   // This parameter is represented from Note26
**********************************************************************************
```

```
*********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN   // This parameter is represented from Note27
#define byte   DOutput1Reg   // This parameter is represented from Note28
#define byte   DOutput1Bit   // This parameter is represented from Note29
#define byte   DOutput1Val   // This parameter is represented from Note30
#define byte   DOutput2LDN   // This parameter is represented from Note31
#define byte   DOutput2Reg   // This parameter is represented from Note32
#define byte   DOutput2Bit   // This parameter is represented from Note33
#define byte   DOutput2Val   // This parameter is represented from Note34
#define byte   DOutput3LDN   // This parameter is represented from Note35
#define byte   DOutput3Reg   // This parameter is represented from Note36
#define byte   DOutput3Bit   // This parameter is represented from Note37
#define byte   DOutput3Val   // This parameter is represented from Note38
#define byte   DOutput4LDN   // This parameter is represented from Note39
#define byte   DOutput4Reg   // This parameter is represented from Note40
#define byte   DOutput4Bit   // This parameter is represented from Note41
#define byte   DOutput4Val   // This parameter is represented from Note42
#define byte   DOutput5LDN   // This parameter is represented from Note43
#define byte   DOutput5Reg   // This parameter is represented from Note44
#define byte   DOutput5Bit   // This parameter is represented from Note45
#define byte   DOutput5Val   // This parameter is represented from Note46
#define byte   DOutput6LDN   // This parameter is represented from Note47
#define byte   DOutput6Reg   // This parameter is represented from Note48
#define byte   DOutput6Bit   // This parameter is represented from Note49
#define byte   DOutput6Val   // This parameter is represented from Note50
#define byte   DOutput7LDN   // This parameter is represented from Note51
#define byte   DOutput7Reg   // This parameter is represented from Note52
#define byte   DOutput7Bit   // This parameter is represented from Note53
#define byte   DOutput7Val   // This parameter is represented from Note54
#define byte   DOutput8LDN   // This parameter is represented from Note55
#define byte   DOutput8Reg   // This parameter is represented from Note56
#define byte   DOutput8Bit   // This parameter is represented from Note57
#define byte   DOutput8Val   // This parameter is represented from Note58
*********************************************************************************
```

```
*****************************************************************************************
VOID   Main(){
       Boolean PinStatus ;

       // Procedure : AaeonReadPinStatus
       // Input :
       //      Example, Read Digital I/O Pin 3 status
        // Output :
        //      InputStatus :
        //              0: Digital I/O Pin level is low
        //              1: Digital I/O Pin level is High
       PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

       // Procedure : AaeonSetOutputLevel
       // Input :
       //      Example, Set Digital I/O Pin 6 level
       AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*****************************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(LDN, Register, BitNum);
        Return PinStatus ;
}
VOID    AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
        ConfigToOutputMode(LDN, Register, BitNum);
        SIOBitSet(LDN, Register, BitNum, Value);
}
*****************************************************************************
```

```
*******************************************************************************
VOID   SIOEnterMBPnPMode(){
       IOWriteByte(SIOIndex, 0x87);
       IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*******************************************************************************
```

```
*****************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, Register);
         TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID    ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
        Byte TmpValue, OutputEnableReg;

        OutputEnableReg = Register-1;
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, OutputEnableReg);
         TmpValue = IOReadByte(SIOData);
         TmpValue |= (1 << BitNum);
         IOWriteByte(SIOData, OutputEnableReg);
         SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix D

Glue Removal Procedure

D.1 Removing Glue from Your System

To protect components from damage and ensure proper operation out of the box, glue may have been applied to some cables or connectors to keep them in place during shipping. This glue must be removed before attempting to swap components or perform maintenance. This section details the steps needed to remove the glue.

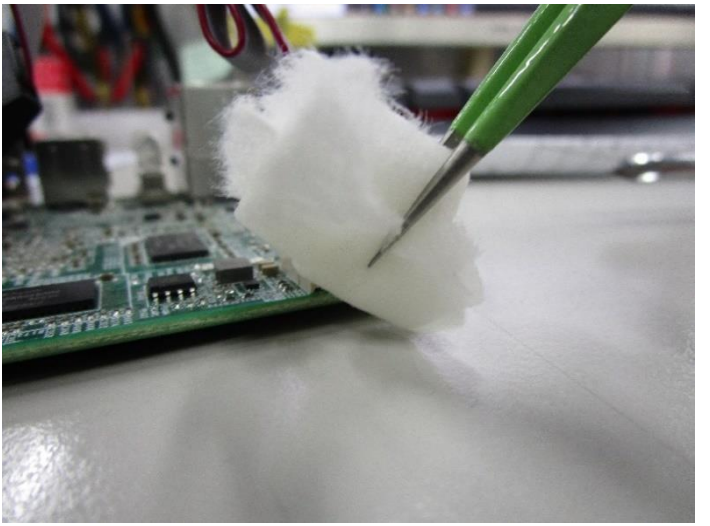
Before performing any kind of system maintenance, ensure the system is shut down (not in sleep or hibernate mode) and the power cable has been removed. Follow steps in Chapter 2 to access the components inside.

You will need the following items for this step:

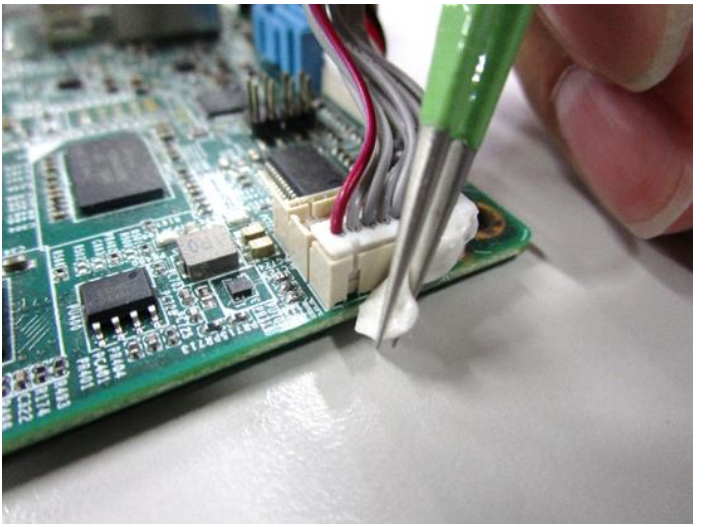
- Cotton or cotton swab
- Anti-static tweezers
- An alcohol solution that is at least 99.5% alcohol (ethanol solution or denatured alcohol). AAEON recommends using an eye dropper or a bottle with a nozzle as in the picture below:

Step 1: Using an eyedropper or bottle as shown above, apply a few drops of alcohol to the glue.

Step 2: Allow the alcohol to soak for 10 seconds, then use a cotton swab or cotton with anti-static tweezers to evenly rub the alcohol over the glue.



Step 3: Let soak for 10 more seconds, then use anti-static tweezers to remove the glue.



If you encounter any issues or need support, please contact your AAEON representative or visit our Support Page at AAEON.com